

# Technical Datasheet

# Graphene Field-Effect Transistor Chip: mGFET 4x4P

## **General Description**

The mGFET 4x4 chip from Graphenea is designed for sensing applications, and it is compatible with measurements in a liquid medium. The metal pads are passivated to avoid degradation and reduce leakage currents. It also includes a non-encapsulated electrode at the center of the chip, which allows for liquid gating without the need of an external gate electrode (such as Ag/AgCl probes). This device architecture enhances signal-to-noise ratio and reduces parasitics.

This version provides 28 graphene graphene channels: 7 of them are one-channel devices and 7 of them are three-channel devices. These two geometries add flexibility to the measurement scheme ( $\Delta V_D$  or  $\Delta I_{sd}$ ). The die is packaged and wirebonded to a leadless chip carrier (LCC) and it is fully compatible with the Graphenea Card.

### Features

- State-of-the-art GFETs utilizing Graphenea's established consistently high-quality graphene
- Semiencapsulated geometry + central gate electrode for measurements in liquid environments.
- Packaged die for easy integration into readout schemes.
- 7x one-channel + 7x three-channel devices per chip.
- Mobilities typically in excess of 1000 cm<sup>2</sup>/V·s

Applications

- Graphene device research
- Chemical/gas sensing
- Biosensors
- Chemical sensors
- Bioelectronics
- Healthcare
- Industrial safety

## **Typical Specifications**

Die dimensions	4 mm x 4 mm
Chip thickness	525 μm
Number of channels per chip	28
Gate Oxide thickness	90 nm
Gate Oxide material	SiO <sub>2</sub>
Resistivity of substrate	1-10 Ω·cm
Metallization	Au contacts
Encapsulation	200 nm Glutarimide-based polymer
Graphene field-effect mobility	>1000 cm <sup>2</sup> /V·s
Dirac point (liquid gating in PBS)	<1 V
Yield	>75 %

### Absolute Maximum Ratings

Maximum gate-source voltage (liquid gating in PBS)	± 2V
Maximum temperature rating	150 °C
Maximum drain-source current density	10 <sup>7</sup> A·cm <sup>-2</sup>



miniGFET 4x4P Layout



#### **Device cross-section**



#### **Typical characteristics**



(a) Output curve, measured at room temperature and vacuum conditions. (b) Transfer curve measured at source-drain voltage of 20mV under liquid gating through Phosphate Buffered Saline (PBS, pH=7.3), using the on-chip electrode as gate electrode.

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Die to carrier Layout



LCC dimensions (inches)



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# LCC specifications

LCC Model	SSM P/N LCC02034
Standard	JEDEC Type C
Number of pads	20
Body material	Ceramic and black alumina
Contact material	Ni + Au plated

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